REMARKS

Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

Claims 1-3 stand rejected under 35 U.S.C. 102(e) as being anticipated by Kojima (U.S. 6,072,241). This ground of rejection is respectfully traversed.

Our claimed inventions differ significantly from the disclosure of Kojima in several respects. The device isolation film of Kojima is a conventional one and does not have a groove or an opening. The gate electrode structure of the present invention comprises a first and a second gate electrode, wherein the first gate electrode has the same height as the device isolation film. The gate electrode of Kojima includes a stacked structure which is a conventional one. The spacer of the present invention is formed on the side wall of the first gate electrode and on the side wall of the device isolation film. The spacer of Kojima is formed on the entire side wall of gate electrode, not on a portion of the side wall.

In view of the foregoing, the claims are now believed to be in form for allowance, and such action is hereby solicited. If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

Attached is a marked-up version of the changes made to the specification and claims by the current amendment. The attached Appendix is captioned **"Version with markings to show changes made"**.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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APPENDIX VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

1. (Amended) A transistor comprising:

a device isolation [oxide] film formed on a semiconductor substrate, the device isolation [oxide including an opening] film having a groove therein that exposes a portion of the semiconductor [substrate, the exposed portion of the semiconductor] substrate defining an active [region] region and having substantially vertical profile with respect to the exposed portion of the semiconductor substrate;

a gate electrode structure formed in the [active region, wherein the gate electrode structure covers only a] central portion of the active [region and is] region, separated from the device isolation [oxide] film, [the gate electrode structure further comprising]

wherein the gate electrode structure comprises:

a stacked structure of a gate oxide film, a first gate electrode and a second gate electrode being formed on the semiconductor [substrate in the active region,] substrate;

[a gate electrode formed on the gate oxide film, the gate electrode having an upper surface and two substantially vertical sidewalls,

the gate electrode further comprising a stacked structure having a first conductor and a second conductor,]

an oxide layer formed on [the first conductor,] a side wall of the first gate electrode; and

[nitride spacers] a first nitride spacer formed on the oxide layer [on the sidewalls of the gate electrode];

a second nitride spacer formed on the oxide layer;

lightly doped drain (LDD) regions formed in the active region of the semiconductor substrate on both sides of the gate electrode;

source/drain regions formed in the active region of the semiconductor substrate on both sides of the gate electrode; and

second and third insulating films filling and planarizing the space above the active region and between the gate electrode structure and the [device isolation oxide film.] second nitride spacer.

2. (Amended) The transistor according to claim 1, wherein the [device isolation oxide film surrounding the opening has substantially vertical profile with respect to the exposed portion of the semiconductor substrate,]

[the profile being modified] groove has a rounded profile near the junction of the device isolation [oxide] film and the semiconductor substrate [such that the device isolation oxide film has a substantially rounded profile].

3. (Amended) The transistor according to claim 1, [wherein] further comprising a hard mask layer [is formed] on the gate electrode structure.

End of Appendix